



Register content and address map

The OPN register is provided with the internal address as shown in the address map. The content of each register (address) is as follows.

(1)	\$00 ~ \$05	Generates frequency of the square wave sound source.
(2)	\$06	Generates frequency of noise source.
(3)	\$07	Controls the input and output of the input and output ports and the output of musical sound and noise.
(4)	\$08 ~ \$0A	Controls sound volume. It is possible to select the fixed sound volume system (programmable) or the variable sound volume system.
(5)	\$0B ~ \$0C	Controls the envelope cycle in the variable sound volume system.
(6)	\$0D	Specifies the envelope shape in the variable sound volume system.
(7)	\$0E ~ \$0F	8 bit general-purpose input and output ports.
(8)	\$21	Test information, always set to "0".
(9)	\$24 ~ \$26	Gives the set time of Timers A and B.
(10)	\$27	Controls the operation of Timers A and B, and sets the third channel mode of the FM sound source.
(11)	\$2D ~ \$2F	Specifies the dividing number of the input clock. The dividing numbers 2 through 6 are for the FM sound source, and the numbers 1 through 4 are for square wave sound source.
(12)	\$30 ~ \$3E	Controls Detune and Multiple. This is used to set tones. This controls the relationship between the fundamental wave and harmonic.
(13)	\$40 ~ \$4E	Gives the total level. This information becomes the modulation index of the sound volume and modulation wave of the modulated wave.
(14)	\$50 ~ \$5E	Key - Scale controls the rate of change of A - D - S and R according to the keyboard information. Attack rate gives the rate of change of the envelope at the time of attack.
(15)	\$60 ~ \$6E	Decay Rate shows the rate of change of the envelope at the time of decay.
(16)	\$70 ~ \$7E	Sustain Rate shows the rate of change of the envelope at the time of sustain.
(17)	\$80 ~ \$8E	Sustain level shows the level of the shift from decay to sustain. Release rate shows the rate of change of the envelope at the time of release.
(18)	\$90 ~ \$9E	Generates the envelope including the repeat pattern similar to that of square wave sound source.
(19)	\$A0 ~ \$A6	Gives key-code (F-number) of each channel.
(20)	\$A8 ~ \$AE	Gives the key-code (F-number) of three channels when set to the special mode.
(21)	\$B0 ~ \$B2	Gives the modulation system (connection) of the FM modulation and the modulation factor of the feedback FM (self-feedback).

FM system

In the FM system, musical sounds are synthesized by controlling various high harmonic waves by use of the frequency modulation. The basic equation of the FM system is as follows.

waves by use of the frequency modulation. The basic equation of the FM system is as follows.

(Equation 1) $F = A \sin (\omega C t + I \sin \omega M t)$

Where A is output amplitude, I is modulation index, and ωC and ωM are angular frequencies of carrier and modulator, respectively. This equation can also be expressed as follows.

(Equation 2) $F = A [J_0(I) \sin \omega C t + J_1(I) (\sin (\omega C + \omega M)t - \sin (\omega C - \omega M)t) + J_2(I) (\sin (\omega C + 2 \omega M)t - \sin(\omega C - 2 \omega M)t) + \dots]$

Where, $J_n(I)$ is the first class Bessel function of nth As shown in the above equation, the FM system contains various harmonics and can control them. The OPN provides the multiple FM modulation and feedback FM modulation shown in (3) and (4) in addition to the above FM modulation to produce every possible sound.

(Equation 3) $F = A \sin [\omega C t + I_1 \sin (\omega M_1 t + I_2 \sin \omega M_2 t)]$

(Equation 4) $F = A \sin (\omega C t + \beta F)$

WRITE DATA

Address	Data Bits								Comment
21	TEST								LSI TEST DATA
24	TIMER-A								8 most significant bits of TIMER-A
25	not used						TIMER-A		2 least significant bits of TIMER-A
26	TIMER-B								TIMER-B data
27	MODE	RESET B	RESET A	ENABLE B	ENABLE A	LOAD B	LOAD A	TIMER-A/B control and 3 channel mode	
28	SLOT				CH				Key-ON/OFF
2D	don't care								Set pre-scaler
2E	don't care								Selection of the dividing numbers of 1/3 and 1/6
2F	don't care								Set a divider to the dividing number of 1/2
30-3E	not used	DT			MULTI				Detune/Multiple (Addresses 33, 37, 3B are empty)
40-4E	not used	TL							Total Level (Addresses 43, 47, 4B are empty)
50-5E	KS	not used	AR						Key Scale/Attack Rate (Addresses 53, 57, 5B are empty)
60-6E	not used		DR					Decay Rate (Addresses 63, 67, 6B are empty)	
70-7E	not used		SR					Sustain Rate (Addresses 73, 77, 7B are empty)	
80-8E	SL				RR				Sustain Level/Release Rate (Addresses 83, 87, 8B are empty)
90-9E	not used				SSG-EG				SSG-Type Envelope Control (Addresses 93, 97, 9B are empty)
A0-A2	F-Num. 1								F-Numbers/BLOCK
A4-A6	not used	BLOCK			F-Num. 2				
A8-AA	3CH * F-Num. 1								3CH-3slot
AC-AE	not used	3CH * BLOCK			3CH * F-Num. 2				F-Numbers/BLOCK
B0-B2	not used	FB			CONNECT				Self-Feedback/Connection

B0-B2	not used	FB	CONNECT	Self-Feedback/Connection
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READ/WRITE DATA

Address	Data Bits				Comment	
00	Fine Tune				Channel-A Tone Period	
01	not used	Coarse Tune				
02	Fine Tune				Channel-B Tone Period	
03	not used	Coarse Tune				
04	Fine Tune				Channel-C Tone Period	
05	not used	Coarse Tune				
06	not used	Period Control			Noise Period	
07	IN/OUT IOB	IN/OUT IOA	_NOISE	_TONE	_ENABLE	
08	not used	M	Level		Channel-A Amplitude	
09	not used	M	Level		Channel-B Amplitude	
0A	not used	M	Level		Channel-C Amplitude	
0B	Fine Tune				Envelope Period	
0C	Coarse Tune					
0D	not used	C	ATT	ALT	HLD	Envelope Shape/Cycle
0E	I/O Port-A				I/O Port Data	
0F	I/O Port-B					

READ DATA

Address	Data Bits				Comment
xx	BUSY	not used	FLAG B	FLAG A	Status

• ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

ITEM	RATING	UNIT
Terminal voltage	-0.3 ~ 7.0	V
Ambient operating temperature	0 ~ 70	°C
Storage temperature	-50 ~ 125	°C

2. Recommended Operation Conditions

ITEM	SYMBOL	MIN.	STD.	MAX.	UNIT
Supply voltage	Vdd	4.75	5.0	5.25	V
	Vss	0	0	0	V

3. DC Characteristics

ITEM	SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Input high level voltage	Total input	V _{IH}	2.0		V _{DD}	V
Input low level voltage	Total input	V _{IL}	-0.3		0.8	V
Input leakage current	øM, _WR, _RD, A0	I _L	V _{in} = 0 ~ 5V	-10	10	µA
Three-state (off) input current	D0 ~ D7	I _{TSL}	V _{in} = 0 ~ 5V	-10	10	µA
Output high level voltage	Output except _IRQ	V _{OH1}	I _{OH1} = 0.4mA	2.4		V
		V _{OH2}	I _{OH2} = 40µA	3.3		V
Output leakage current (off)	_IRQ	I _{OL}	V _{OH} = 0 ~ 5V	-10	10	µA
Analog output voltage	ANALOG-CHA, B, C	V _{OA}	Max. Sound volume, no mixing	0.95	1.35	V _{pp}
Power current		I _{DD}			120	µA

voltage	C	VOA	volume, no mixing	0.95		1.35	V _{pp}
Power current		IDD				120	mA
Pull-up resistance	IOA0 ~ IOA7, IOB0 ~ IOB7, _IC, _CS	R _{PU}		60		600	k
Input capacitance	Total input	C _I	f = 1MHz			10	pF
Output capacitance	Total output	C _O				10	pF

4. AC Characteristics

ITEM		SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Input clock frequency	∅M	f _c	Pre-scaler function (Fig. A-1)	0.7		4.2	MHz
Input clock duty	∅M			40	50	60	%
Input clock rise time	∅M	T _R	(Fig. A-1)			50	ns
Input clock breaking time	∅M	T _F	(Fig. A-1)			50	ns

5. Access to FM sound source

ITEM		SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Address set-up time	A0	T _{AS}	(Figs. A-2 and A-3)	10			ns
Address hold time	A0	T _{AH}	(Figs. A-2 and A-3)	10			ns
Chip select write width	_CS	T _{CSW}	(Fig. A-2)	200			ns
Chip select read width	_CS	T _{CSR}	(Fig. A-3)	250			ns
Write pulse write width	_WR	T _{WW}	(Fig. A-2)	200			ns
Write data set-up time	D0 ~ D7	T _{WDS}	(Fig. A-2)	100			ns
Write data hold time	D0 ~ D7	T _{WDH}	(Fig. A-3)	20			ns
Read pulse width	_RD	T _{RW}	(Fig. A-3)	250			ns
Read data access time	D0 ~ D7	T _{ACC}	C _L = 100pF (Fig. A-3)			250	ns
Read data hold time	D0 ~ D7	T _{RDH}	(Fig. A-3)	10			ns
Output rise time	∅S	T _{OR1}	C _L = 100pF (Fig. A-4)			200	ns
	OP-O, SH	T _{OR2}	C _L = 100pF (Fig. A-5)			300	ns
Output rise time	∅S	T _{OF1}	C _L = 100pF (Fig. A-4)			200	ns
	OP-O, SH	T _{OF2}	C _L = 100pF (Fig. A-5)			300	ns

6. Access to SSG sound source

ITEM		SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Address set-up time	A0	T _{SAS}	(Figs. A-7 and A-8)	10			ns
Address hold time	A0	T _{SAH}	(Figs. A-7 and A-8)	10			ns
Chip select write width	_CS	T _{SCSW}	(Fig. A-7)	250			ns
Chip select read width	_CS	T _{SCSR}	(Fig. A-8)	400			ns
Write pulse write width	_WR	T _{SWW}	(Fig. A-7)	250			ns
Write data set-up time	D0 ~ D7	T _{SWDS}	(Fig. A-7)	0			ns
Write data hold time	D0 ~ D7	T _{SWDH}	(Fig. A-7)	20			ns

Write data set up time	D0 ~ D7	T _{SWDS}	(Fig. A-7)	0			ns
Write data hold time	D0 ~ D7	T _{SWDH}	(Fig. A-7)	20			ns
Read pulse width	_RD	T _{SRW}	(Fig. A-8)	400			ns
Read data access time	D0 ~ D7	T _{SACC}	CL = 100pF (Fig. A-8)			400	ns
Read data hold time	D0 ~ D7	T _{SRDH}	(Fig. A-8)	10			ns

ITEM	SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Reset pulse width	_IC T _{ICW}	(Fig. A-9)	73*			cycle

* Depends on the dividing number of prescaler. Pulse width = (dividing number) x 12

• TIMING DIAGRAM

(Timing is set on the basis of the values: V_{IH} = 2.0V and V_{IL} = 0.8V).

- **Fig. A-1 Clock Timing**
(figure not available online)
- **Fig. A-2 FM section write timing**
(figure not available online)
Note. T_{CSW}, T_{WW} and T_{WDH} are determined based on the time when either _CS or _WR goes to the high level.
- **Fig. A-3 FM section read timing**
(figure not available online)
Note. T_{AAC} is determined based on the time when either _CS or _RD goes to the low level. T_{CSR}, T_{RW} and T_{RDH} are determined based on the time when either _CS or _RD goes to the high level.
- **Fig. A-4 -a øM and øS (dividing numbers: 2 and 3)**
(figure not available online)
- **Fig. A-4-b øM and øS (dividing number: 6)**
(figure not available online)
- **Fig. A-5 øM and SH . OP-O**
(figure not available online)
- **Fig. A-6 Timing of øS and OP-O/CH at each dividing number**
(figure not available online)
- **Fig. A-7 SSG section write timing**
(figure not available online)
Note. T_{SWDS} is determined based on the time when either _CS or _WR goes to the low level. T_{SCW}, T_{SWW} and T_{SWDH} are determined based on the time when either _CS or _WR goes to the high level.
- **Fig. A-8 SSG section read timing**
(figure not available online)
Note. T_{SACC} is determined based on the time when either _CS or _RD goes to the low level. T_{CSR}, T_{SRW} and T_{SRDH} are determined based on the time when either _CS or _RD goes to the high level.
- **Fig. A-9 Reset pulse**
(figure not available online)