Apple II Digital Storage Oscilloscope

Use minimal hardware, Applesoft BASIC, and 6502 machine language to convert an Apple II into a triggered digital "storage oscilloscope."

This article gives complete details on building a peripheral card that fits in slot #7 of the Apple II computer. The card has an audio frequency buffer and attenuation circuit, plus a very easy-to-use analog-to-digital converter which is capable of sampling the signal every 25 microseconds. The software is a combination program of Applesoft BASIC and 6502 machine language. It prompts you to initiate an audio input, then waits for it. It has a trigger threshhold. When the signal level exceeds the threshhold, the circuit takes 19,600 samples spaced about 40 μS apart, storing each one in upper RAM (starting at $7370 in a 48K space). Then a high-resolution plot of the first 280 samples — one screen — is displayed.

The caption beneath the screen-plot gives start and stop times of that screen in milliseconds. It also prompts you to push certain keys to look at other screen-plots. There are 70 screen-plots altogether, each covering roughly 12 milliseconds. Thus, the original signal is sampled for about .84 seconds. See figure 1 for an example of a screen-plot. The circuitry and code are fully operational, but the information here should really be taken as a suggestive guide for customizing the ideas to your own needs.

Physically, the circuit is connected together by point-to-point soldering of wire-wrap type wire on a California Computer Systems model 7500 prototype board (see figure 2). (This board costs $21, and the labels on both sides

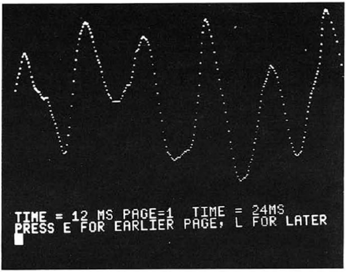

Figure 1: Sample plot of waveform produced by a conga drum.

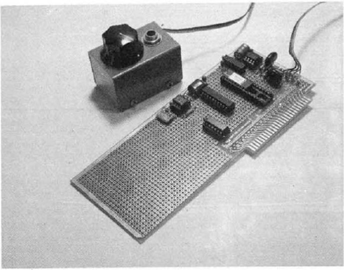

Figure 2: Component side of the ADC board.

for all edge-connector terminals are very helpful for wiring and checkout.) There is a two-wire ribbon cable from the card to a little metal box with a phone jack for plugging in the signal, and a potentiometer for attenuating the input signal.

You do well if you find an integrated circuit as friendly as the Analog Devices AD570JD. This costs $22 (in singles) but is a completely self-contained, successive-approximation, analog-to-digital converter. It has one analog input (choose unipolar 0-10V input by grounding the BIPOLAR CONTROL pin, or leave the pin floating for bipolar + − 5V input), and 8 digital outputs. There is one input control line called BLANK/$\overline{\text{CONVERT}}$ (B/$\overline{\text{C}}$), and one output acknowledgement line, $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$). In BLANK mode the digital output lines are floated (tri-state, high impedance condition). Nothing happens until B/$\overline{\text{C}}$ is brought low, thereby switching the unit into CONVERT mode. After grinding out the answer in 25 μS, the result appears latched onto the eight output lines, and DR is brought low. That is it. Bring the unit back into BLANK, and start over. It has to stay in BLANK a minimum of 2 μS before another conversion is initiated. Also, in bipolar mode the output is offset binary (zero signal gives output 128). At this point you can foresee that the software loop for filling RAM area with samples of audio signal will have the following steps:

1. initiate a conversion by bringing B/$\overline{\text{C}}$ from low to high for 2 μS;
2. wait at least 25 μS, and use the time to check for done and to compute the address of the next location to stick the answer;
3. read the answer;
4. stick it in RAM;
5. go back to 1.

Here is how the circuit works (figure 3). The audio signal is applied at phonejack J1 to a non-inverting gain stage based on a 741-type operational amplifier. Potentiometer P1 adjusts input signal level, and is mounted remotely with J1. The gain is equal to one plus the ratio of R2 to R1, and with the values shown, the gain is 7.8. The back-to-back Zener diodes Z1, Z2 clip the signal to + − 5V peak-to-peak, which is the analog input range of the AD570JD.

I needed a 2 μS positive-going pulse from some pin of slot #7. That was not available, but the DEVICE SELECT line at pin 41 of the peripheral connector "becomes active (low)... when the address bus is holding an address between $C0n0 and $C0nF, where n is the slot number plus $8." This specification (*Apple II Reference Manual*, p. 109) determines the choice of locations $C0F0 and $C0F1 for initiating the conversion, and reading the answer, respectively. The 74LS00 quad NAND-gate is the address decoder, and either triggers ($C0F0) the 555 one-shot (set for 2 μS by R3, C4), or momentarily puts the

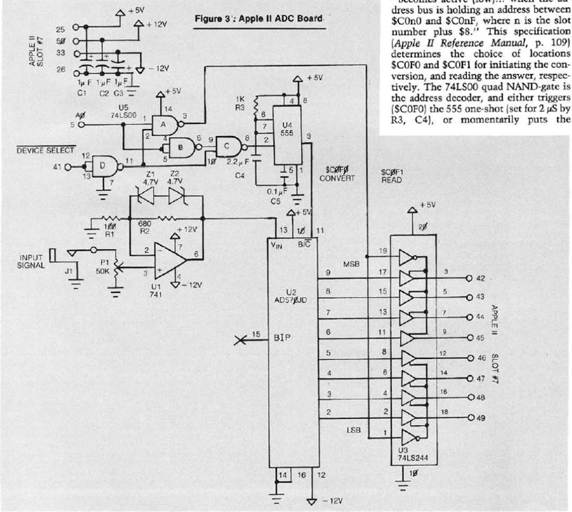

Figure 3: Apple II ADC Board

Listing 1

```
100  HOME
110  REM ---DEFINE UPPER LIMIT OF BASIC AREA;
120  REM ---LOWER LIMIT OF DATA BUFFER;
130  REM ---K IS A CONVERSION CONSTANT
140  REM ---FOR PLOTTING IN HI-RES.
150  HIMEM: 8191:BASE = 29552:W = 159 / 255
160  REM ---PROMPT.
170  PRINT "PLAY A FEW NOTES AFTER HEARING TONE"
180  REM ---BRIEF DELAY.
190  FOR I = 1 TO 500: NEXT
200  REM ---BRIEF TONE.
210  FOR I = 1 TO 200:E =  PEEK (49200): NEXT
220  REM ---DEFINE JMP $0300 FOR USR FUNCTION.
230  POKE 10,76: POKE 11,0: POKE 12,3
240  REM ---CALL DATA COLLECTION ROUTINE.
250 ANS =  USR (X)
260  REM ---INITIALIZE FOR SCREEN-PLOT ("PAGE") CAPTION.
270 TIME = 12:PAGE = 0
280  REM ---INITIALIZE FOR HI-RES:
290 SW = 49232
300  REM ---MIXED,
310  POKE SW + 3,0
320  REM ---PAGE-ONE,
330  POKE SW + 4,0
340  REM ---HIGH-RESOLUTION,
350  POKE SW + 7,0
360  REM ---GRAPHICS.
370  POKE SW,0
380  REM :---ADJUST CURSOR FOR CAPTION.
390  HOME : VTAB 21: POKE 36,0
400  REM ---DISPLAY CURRENT PAGE.
410  GOSUB 560
420  REM ---COMPUTE AND DISPLAY CAPTION.
430 LFT = PAGE * TIME
440 RIT = LFT + TIME
450  PRINT "TIME = "LFT" MS";
460  PRINT  TAB( 14)"PAGE="PAGE;
470  PRINT  TAB( 22)"TIME = "RIT"MS"
480  REM ---INTERPRET PRESSED KEY.
490  PRINT "PRESS E FOR EARLIER PAGE, L FOR LATER"
500  GET K$: IF K$ <  > "E" AND K$ <  > "L" THEN  GOTO 500
510  IF K$ = "E" AND PAGE > 0 THEN PAGE = PAGE - 1: GOTO 390
520  IF K$ = "L" AND PAGE < 30 THEN PAGE = PAGE + 1: GOTO 390
530  GOTO 500
540  REM ---HI-RES SCREEN-PLOT:
550  REM ---INITIALIZE BEGIN AND END BYTES.
560 LO = BASE + PAGE * 280
570 HI = LO + 279
580  REM ---CLEAR PREVIOUS PLOT.
585  HGR
590  REM ---PLOT 280 DATA POINTS FROM BUFFER.
600  FOR I = LO TO HI
610 Y =  PEEK (I)
620 Y =  INT (Y * W)
630  HPLOT I - LO,159 - Y
640  NEXT
650  RETURN
```

latched data at the converter output ($C0F1) onto the system data bus. That is how the circuit works.

While assembling the unit, I was concerned that the 12V would get through a wiring error onto some TTL line — either onto the +5V supply, or onto an address or data line. So I advise you to do at least as much double-checking and testing of the circuit as I did, even before plugging it in without chips. First, perform continuity tests to insure that there are no paths from −12V to +5V; second, see if all pins have "correct" resistance to ground. Third, leave all chips out, and install the board in slot #7. Turn on the Apple II and if it behaves normally, measure voltages at all pins of all sockets on the new unit. Fourth, when you are satisfied again that all is well, turn off the power, pull the board, and install U4, U5.

Fifth, put the board back, re-apply power, check voltages at the installed chips, and if all is well, try the following test program from the machine language monitor:

```
0C00 STA $C0F0
     STA $C0F1
     JMP $0C00
```

Or, for more fun, try the slightly more elaborate

```
100 A=49392:B=A+1:X=
    40/255
110 POKE A,0
120 Y=PEEK(B):P=INT(X*Y)
130 PRINT TAB(P)"*"
140 GOTO 110
```

Be sure to try out the attenuator, P1.

Listing 2

```
                 ;*******************
                 ;*                 *
                 ;* DIGITAL STORAGE *
                 ;*  OSCILLOSCOPE   *
                 ;*                 *
                 ;*  ELLIS COOPER   *
                 ;*                 *
                 ;*******************
                 ;
                 SCOPE  ORG $300

                 ;
0300 48          START  PHA          ;SAVE PROCESSOR
0301 8A                 TXA          ; STATUS ON STACK...
0302 48                 PHA
0303 98                 TYA
0304 48                 PHA
0305 08                 PHP
0306             ;
0306 A96F               LDA #$6F     ;INITIALIZE TWO CONSECUTIVE
                                       BYTES,
0308 854B               STA $4B      ;$4C $4B, IN PAGE ZERO AS
030A A973               LDA #$73     ;POINTER TO DATA BUFFER..
030C 854C               STA $4C
030E 8DF0C0      CNV1   STA $C0F0    ;START A CONVERSION.
0311 A207               LDX #$07     ;DELAY UNTIL END
0313 CA          DELAY  DEX          ; OF CONVERSION.
0314 D0FD               BNE DELAY
0316             ;
0316 ADF1C0             LDA $C0F1    ;READ PULSE AMPLITUDE.
0319 C98C               CMP #$8C     ;IS THRESHHOLD EXCEEDED?
031B 30F1               BMI CNV1
031D             ;
031D A000               LDY #$00     ;YES; CLEAR Y FOR
                                      INDIRECT-INDEXED MODE

031F 8DF0C0      CNV2   STA $C0F0    ;START A CONVERSION
0322 A54C               LDA $4C      ;LAST PAGE OF BUFFER?
0324 C994               CMP #$94
0326 D006               BNE INCR     ;NO.
0328 A54B               LDA $4B      ;YES; LAST BYTE OF LAST PAGE OF
032A C900               CMP #$00     ;OF BUFFER?
032C F015               BEQ EXIT     ;YES.
032E             ;
032E 18          INCR   CLC          ;NO; CLEAR CARRY FOR ADDITION
032F A54B               LDA $4B
0331 6901               ADC #$01     ;INCREMENT THE POINTER...
0333 854B               STA $4B
0335 A54C               LDA $4C
0337 6900               ADC #$00
0339 854C               STA $4C
033B             ;
033B ADF1C0             LDA $C0F1    ;READ PULSE AMPLITUDE
033E 914B               STA ($4B),Y  ;STORE IN DATA BUFFER
0340 4C1F03             JMP CNV2     ;GO BACK FOR MORE
0343             ;
0343 28          EXIT   PLP          ;RESTORE PROCESSOR STATUS
0344 68                 PLA          ;FROM STACK
0345 A8                 TAY
0346 68                 PLA
0347 AA                 TAX
0348 68                 PLA
0349             ;
0349 60                 RTS          ;RETURN TO BASIC.
                        END
```

Using an oscilloscope you should see 2 μS positive pulses at U2(11) and 0.5 μS active-low pulses at U3(1) and U3(19). Now, sixth, install the remaining chips and repeat all tests.

If everything appears OK at this point, you may be confident that your board is working, but there is nothing like a conversion to convince you. Seventh, plug in an electric guitar or a microphone, or even just a speaker which has a big magnet, and try a program in BASIC:

```
100 POKE 49392,0
110 PRINT PEEK(49393)" ";
120 GOTO 100
```

If these little tests do not turn up any surprises, it is time to put in the main program of this article (listing 1 and listing 2). Be sure to save both parts before running. Be warned, you must have 48K RAM to use this software exactly as written. Like I said, though, you should use these listings only as a starting point, if at all, to carry out your own ideas.

One refinement of the software would be to display only every nth sample, or to sample less frequently but for a longer duration. Another idea is to swap back and forth between two high-resolution pages, achieving an "animated" display of the waveform. As for me, it is time to bone up on algorithms for extracting significant information from the stored data, e.g., pitch periods, envelopes, and so forth.

References

1. "The Piecewise-Linear Technique of Electronic Music Synthesis," E.D. Cooper and A.D. Bernstein, *Journal of the Audio Engineering Society*, V. 24, No. 6, July/August, 1976, pp. 446-454.

2. "Circuits for the Piecewise-Linear Technique of Electronic Music Synthesis," E.D. Cooper, *Electronotes Newsletter of the Musical Engineering Group*, V. 8, No. 69, September, 1976, pp. 8-13.

3. "Program Performs Harmonic Analysis," E.D. Cooper, *μComputerist Corner*, EDN, February 5, 1980, pp. 80-85.

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